
450 Mbit/s – 2 Gbit/s Display Transmitter

Features

- Low power operation: 30 mW/lane (typical)
- Supports data rates from 0.45 to 2 Gbit/s
- Utilizes 9-bit parallel interface
- Supports 0 – 7 dB programmable pre-emphasis
- Integrated on-die termination resistors
- DC & AC coupling support
- Lane-to-lane de-skew function
- One independent PLL shared in every macro
- Embedded BIST
- Available in BGA and QFN/QFP packages