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## PCIe 3.0

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### Features

- Standard PHY interface (PIPE) enables multiple IP sources for PCIe 3.0 MAC Layer
- Dual port PIPE with shared REF CLK configurable to be 2-lane PCIe PHY
- Supports 2.5 GT/s and 5.0 GT/s serial data transmission rate
- Supports 16- or 32-bit parallel interface when encoding/decoding enabled
- Supports 20-bit parallel interface when encoding/decoding bypassed
- Supports PCLK as PHY output
- Data and clock recovery from serial stream
- 8b/10b encoder/decoder and error indication
- Supports direct disparity control for use in transmitting compliance pattern

- Supports power change and rate change in same PCLK cycle
- Receiver detection
- Beacon transmission and reception
- Supports transmitting LFPS when power state changes
- Selectable TX margining
- Selectable TX de-emphasis, and signal swing values
- Compliant with PCIe 3.0 specification

### Applications

- PC
- Data Storage
- Multimedia Devices