

# 1.25G – 12.5G SERDES

## Features

- Universal SERDES IP range from 1.25 – 10 Gbit/s
- Half data rate and quadrant data rate support
- 40-bit parallel data bus
- Independent channel power down
- Programmable transmit amplitude and TAP configurable FFE in transmitter
- Build in self test with multiple pattern generation and checking for production test
- Integrated on-die termination resistors
- Receiver detection support

- OOB signal generation and detection support
- Spread Spectrum clock generation (optional) and receive support
- Flexible reference clock frequency, 25 – 156.25 MHz
- Support  $\times 1$ ,  $\times 2$ ,  $\times 4$  lanes
- No external component
- ESD: HBM/MM/CDM/Latch Up 2 kV/200 V/500 V/100 mA

## Applications

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## Block Diagram:

