USB 2.0 UTMI+ lvl3 PHY

Features

• SMIC 40 nm low leakage 6 metal process
• Ultra low area:
  <0.06 mm² excluding OTG and I/O pads
  <0.065 mm² including OTG but excluding I/O pads
• Ultra low power, typically:
  30 mW during HS-transmission
  7 mW during HS-receive
  5 mW during HS-idle
• Extensive built in self test for production testing
• UTMI+ level 3 compliant
• Internal reference resistor that automatically re-
  places the external reference resistor if no external
  resistor has been connected
• One control bit DP/DM polarity inversion for sim-
  plified PCB signal routing both for top and bottom
  mounted connectors
• Supports 4, 8, 12, 20, 25, 40, 50 and 100 MHz reference
  clock frequencies