USB 3.0 PHY

Features

• Standard PHY interface (PIPE) enables multiple IP sources for USB 3.0 Link Layer
• Supports 5.0 GT/s serial data transmission rate
• Supports 16- or 32-bit parallel interface
• Supports PCLK as PHY output
• Data and clock recovery from serial stream
• 8b/10b encoder/decoder and error indication
• Receiver detection
• Low Frequency Period Signalling (LFPS) transmission and reception
• Supports transmitting LFPS when power state changes
• Selectable TX margining
• Compliant with USB 3.0 specification
• TSMC 28/TSMC 40/SMIC 40/SMIC 0.13 nm processes

Applications

• All USB devices

Block Diagram:

[Diagram showing the components of the USB 3.0 PHY, including TXONESZEROS, TXDATA[31:0], TXDATAK, RXDATA[31:0], RXVALID, RXSTATUS[2:0], PHYSTATUS, RXELECIDLE, LFPS & Other, 8b/10b Encoder, MUX, RX Detect, TX +/-, 10b/8b Decoder, FIFO, CDR, RX +/-, SKP/Comma Detector & Word Alignment, LFPS Detector, PHY/RX Status, FIFO, and MUX.]