PCIe/USB/SATA Combo PHY

Features

- Standard PHY interface (PIPE) enables multiple IP sources for PCIe/USB/SATA MAC Layer
- Dual port PIPE with shared REF_CLK configurable to be 2-lane PCIe PHY
- Supports 2.5 GT/s and 5.0 GT/s serial data transmission rate in PCIe mode
- Supports 5.0 GT/s serial data transmission rate in USB mode
- Supports 1.5 GT/s, 3.0 GT/s and 6.0 GT/s serial data transmission rate in SATA mode
- Supports 16- or 32-bit parallel interface when encoding/decoding enabled
- Supports 20-bit parallel interface when encoding/decoding bypassed
- Supports PCLK as PHY output
- Data and clock recovery from serial stream
- 8b/10b encoder/decoder and error indication
- Supports direct disparity control for use in transmitting compliance pattern in PCIe mode
- Supports power change and rate change in same PCLK cycle in PCIe/SATA mode
- Receiver detection in PCIe/USB mode
- Beacon transmission and reception in PCIe mode
- Low Frequency Periodic Signaling (LFPS) transmission and reception in USB mode
- COMWAKE, COMINIT and COMRESET (OOB) transmission and reception in SATA mode
- Supports transmitting LFPS when power state changes
- Selectable TX margining in PCIe/USB mode
- Selectable TX de-emphasis, and signal swing values in PCIe mode
- Compliant with PCIe/USB/SATA base specification

Applications

- PC
- Data Storage
- Multimedia Devices