eDP 1.4 Transmitter

Features
- Compliant with Embedded DisplayPort 1.4 specification
- Main Link supports 1, 2 or 4 lanes at 1.62Gbps, 2.7Gbps and 5.4Gbps
- 4 channel S/PDIF Digital Audio Input
- Supports Enhanced Framing Mode
- Automatic Link-Training with option of firmware-controlled Link-Training procedure
- Supports Fast Link Training
- Supports AUX Channel for Access of DPCD and EDID
- Supports Deep-Color up to 48-bit RGB/YCbCr Digital Video Transport
- Supports Advanced Link Power Management
- Supports GTC function
- Supports Panel Self Refresh function

Applications
- LCD TV
- HDTV
- Projectors
- Legacy Converter

Block Diagram:

- Crystal Clock
- TEST_CLK
- DE
- VSYNC
- HSYNC
- VD[47:0]
- PIX_CLK
- SPDIF x 4
- FS512_CLK
- Audio I/F
- Video I/F
- Video TBC
- Video Packer
- Secondary Data Packer
- InfoFrame Ports, TimeStamp Port
- MUX & BS/BE/RS Insertion
- M.S. Attributes
- Training Pattern Generator
- 8/10 Encoder/Scrambler
- 4x8
- Serializer
- Link Training Controller (FSM)
- AUG (M-II)
- PLL (SSCG)
- HPD_IRQ
- AUX +/-
- CH0 +/-
- CH1 +/-
- CH2 +/
- CH3 +/
- i²c Slave
- i²c Register

Copyright © 2015 | Nano Silicon Pty. Ltd.  http://www.nanosi.com/  A key analog and mixed signal IP provider