

LVDS - Receiver

- LCD-Panel,
- Lap Top PC

NANO SILICON

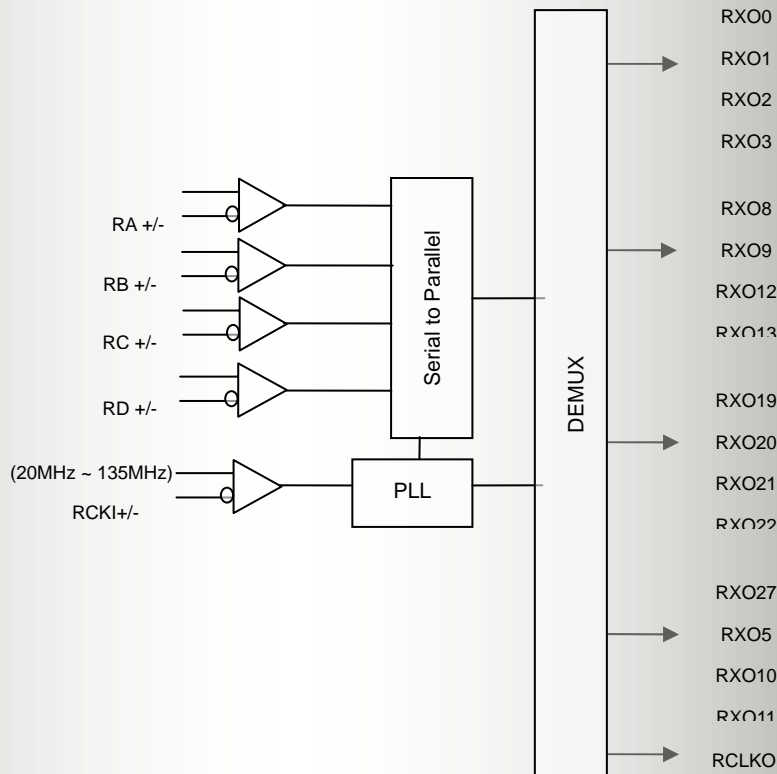
A key analogue and mixed signal IP Provider

LVDS - Receiver



Features

- SMIC 0.18um Process
- TIA/EIA-644 and IEEE 1596.3 Standard Compliant
- Voltage: 1.5V ~ 2.1V
- Input clock frequency: 20 to 135MHz
- Data Bit Rate up to 945Mbps
- PLL requires no external components
- Input Clock Detection with 50MHz Clock output when no input clock detected
- Supports SSCG modulated clock input for EMI reduction (200KHz +/-2.5%)
- Maximum Current at 85MHz < 25mA
- Area < 0.7mm²



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